AMENDMENTS TO THE CLAIMS

1. (Original) A computer-implemented method for run-time reconfiguration of a programmable logic device (PLD) that is coupled to a host data processing arrangement, the host configured with a run-time reconfiguration programming interface, comprising:

executing on the host arrangement a run-time reconfiguration program that, via the programming interface, specifies a circuit design, generates configuration data that implements the circuit design on the PLD, and configures the PLD with the configuration data;

saving a copy of the configuration data on the host arrangement via the programming interface;

activating the PLD;

updating selected portions of the configuration data via the programming interface;

designating portions of the configuration data changed in the updating step as dirty portions by the programming interface; and

automatically selecting the dirty portions of the configuration data by the programming interface for partially reconfiguring the PLD responsive to the run-time reconfiguration program.

2. (Currently Amended) The method of claim 1, further comprising in response to a programming interface call made by the run-time reconfiguration program:

reading back selected portions of configuration data from the PLD as readback data;

updating the copy of the configuration data on the host arrangement with the readback data;

designating portions of the copy of the configuration data changed with the readback data as clean portions; and

in subsequent ~~subsequently~~ partial reconfiguration of the PLD, bypassing the clean portions in selecting configuration data for the PLD.

3. (Original) The method of claim 2, further comprising in response to a programming interface call made by the run-time reconfiguration program:

reading from a designated source configuration data corresponding to selected programmable portions of the PLD, wherein the configuration data from the designated source is read-in data;

updating the copy of the configuration data on the host arrangement with the read-in data; and

designating portions of the copy of the configuration data changed with the read-in data as dirty portions.

4. (Original) The method of claim 3, further comprising in response to a programming interface call made by the run-time reconfiguration program:

selecting the dirty portions from the copy of the configuration data;

assembling one or more packets, each packet containing a configuration command and at least one of the dirty portions; and

transmitting the one or more packets to the PLD.

5. (Original) The method of claim 4, wherein the PLD includes a plurality of configurable logic blocks (CLBs) and is partially configurable in units of one or more frames, each frame including a plurality of CLBs, further comprising establishing a dirty frame map in memory of the host arrangement, wherein a value of each entry in the map indicates whether a corresponding frame of the PLD is dirty.

6. (Original) The method of claim 1, further comprising in response to a programming interface call made by the run-time reconfiguration program:

reading from a designated source configuration data corresponding to selected programmable portions of the PLD, wherein the configuration data from the designated source is read-in data;

updating the copy of the configuration data on the host arrangement with the read-in data; and

designating portions of the copy of the configuration data changed with the read-in data as dirty portions.

7. (Original) The method of claim 6, further comprising in response to a programming interface call made by the run-time reconfiguration program:

selecting the dirty portions from the copy of the configuration data;

assembling one or more packets, each packet containing a configuration command and at least one of the dirty portions; and

transmitting the one or more packets to the PLD.

8. (Original) The method of claim 7, wherein the PLD includes a plurality of configurable logic blocks (CLBs) and is partially configurable in units of one or more frames, each frame including a plurality of CLBs, further comprising establishing a dirty frame map in memory of the host arrangement, wherein a value of each entry in the map indicates whether a corresponding frame of the PLD is dirty.

9. (Original) The method of claim 1, further comprising in response to a programming interface call made by the run-time reconfiguration program:

selecting the dirty portions from the copy of the configuration data;

assembling one or more packets, each packet containing a configuration command and at least one of the dirty portions; and

transmitting the one or more packets to the PLD.

10. (Original) The method of claim 9, wherein the PLD includes a plurality of configurable logic blocks (CLBs) and is partially configurable in units of one or more frames, each frame including a plurality of CLBs, further comprising establishing a dirty frame map in memory of the host arrangement, wherein a value of each entry in the map indicates whether a corresponding frame of the PLD is dirty.

11. (Canceled)

12. (Original) An apparatus for run-time reconfiguration of a programmable logic device (PLD) that is coupled to a host data processing arrangement, comprising:

means for executing a run-time reconfiguration program that includes executable code that specifies a circuit design, generates configuration data that implements the circuit design on the PLD, and configures the PLD with the configuration data;

means for saving a copy of the configuration data on the host arrangement;

means for activating the PLD;

means for updating selected portions of the configuration data via execution of the run-time reconfiguration program;

means for designating updated portions of the configuration data as dirty portions; and

means for automatically selecting the dirty portions of the configuration data for partially reconfiguring the PLD responsive to the run-time reconfiguration program.

13. (Original) A run-time reconfigurable processor arrangement, comprising:

a programmable logic device; and

a host data processing arrangement coupled to the programmable logic device and configured with a run-time reconfiguration program and a run-time reconfiguration programming interface, wherein the run-time reconfiguration program includes executable code that invokes the programming interface to specify a circuit design, generate configuration data that implements the circuit design on the PLD, and configures the PLD with the configuration data; and

wherein the programming interface is further configured, responsive to calls from the run-time reconfiguration program, to save a copy of the configuration data, activate the PLD, update selected portions of the configuration data, designate updated portions of the configuration data as dirty portions, and automatically select the dirty portions of the configuration data for partially reconfiguring the PLD.

14. (Original) The arrangement of claim 13, wherein the programming interface is further configured, responsive to calls from the run-time reconfiguration program, to read back selected portions of configuration data from the PLD as readback data, update the copy of the configuration data on the host arrangement with the readback data, designate portions of the copy of the configuration data changed with the readback data as clean portions; and bypass the clean portions in selecting configuration data for the PLD in subsequent partial reconfiguration of the PLD.

15. (Original) The arrangement of claim 13, wherein the programming interface is further configured, responsive to calls from the run-time reconfiguration program, to read from a designated source configuration data corresponding to selected programmable portions of the PLD, wherein the configuration data

from the designated source is read-in data, update the copy of the configuration data on the host arrangement with the read-in data, and designate portions of the copy of the configuration data changed with the read-in data as dirty portions.

16. (Original) The arrangement of claim 13, wherein the programming interface is further configured, responsive to calls from the run-time reconfiguration program, to select the dirty portions from the copy of the configuration data, assemble one or more packets, each packet containing a configuration command and at least one of the dirty portions, and transmit the one or more packets to the PLD.

17. (Original) The arrangement of claim 13, wherein the PLD includes a plurality of configurable logic blocks (CLBs) and is partially configurable in units of one or more frames, each frame including a plurality of CLBs, wherein the programming interface is further configured, responsive to calls from the run-time reconfiguration program, to establish a dirty frame map in memory of the host arrangement, wherein a value of each entry in the map indicates whether a corresponding frame of the PLD is dirty.